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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,779	GOPALAKRISHNAN ET AL.	
	Examiner	Art Unit	
	SARAH K. SALERNO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39 and 43-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39 and 43-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment/arguments filed on 5/24/2010 as being acknowledged and entered. By this amendment claims 40-42 are canceled, no claims have been added claims 1-39 and 43-45 are pending and no claims are withdrawn.

The Non-Final rejection of claims 1-39 and 43-45 in the Non-Final office action dated 08/05/2010 are withdrawn based on applicants arguments.

2. First, regarding claims 1-39 and 43-45, it is noted that any limitation in a claim with respect to how a claimed device is intended to be used does not differentiate the claimed device from a prior-art device if the prior-art device teaches all structural limitations in the claims and the functional limitations are found to be inherent in the prior art device. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See *Hewlett-Packard Co. v. Bausch & Lomb Inc.* and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a device claim, and not the patentability of its functions (909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990)). As stated in Best,

> Where the claimed and prior art products are identical or substantially identical in structure or composition, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

3. Second, it is noted that the applicant has burden of proof once the examiner establishes a sound basis for believing that the products of the applicant and the prior art are the same. See *In re Spada*, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1-7, 9-20, 30-39 and 43-45 rejected under 35 U.S.C. 102(b) as being anticipated by Claims rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Akimoto (US PGPub 2002/0117689 of record). Refer to rejections in paragraph 7-9.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-7, 9-20, 30-39 and 43-45 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Akimoto (US PGPub 2002/0117689 of record).

Regarding the grounds of rejection of claims 1-7, 9-20, 30-39 and 43-45 under section 103, see MPEP § 2112, which discusses rejection requirements when functional language is present in the claims and recommends the usage of (§102/ §103) grounds of rejection.

8. Akimoto teaches a semiconductor device, comprising: a multi-region body including a first region (22) dominated by charge carriers of a first polarity that extends to a first junction, a second region (23) dominated by charge carriers of a second polarity, opposite the first polarity, that extends to a second junction, and an intermediate region (24) having an effective length extending from the first junction to the second junction; and a gate (20) located over one of the junctions and laterally offset from the other junction, capacitively-coupled to the body FIG. 1A-1B; [0071-0072]), a control circuit configured to apply a control signal, when the body is reversed biased (Fig. 3A-3B [0076-0091]). Akimoto does not specifically discuss modulating the effective length of the intermediate region to a nonzero value by changing a concentration of carriers in a portion of the intermediate region extending from the second junction and offset from the first junction. Akimoto, however, does teach all aspects of the semiconductor device structure in accordance with the instant claimed invention and modulating the effective length of the intermediate region to a nonzero value by changing a concentration of carries in a portion of the intermediate region extending from the second junction and offset from the first junction is a function that does not affect the structure of the final device. Furthermore, Akimoto's device is capable of performing the claimed functions. For instance, manipulating the bias applied to the gate and diffusion regions of the device taught by Akimoto will result in the modulation of the effective length of the intermediate region as described in the presented claim.

Claim 2: Akimoto teaches the control circuit is further configured to apply the control signal to cause the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state [0071-0091].

Claim 3: Akimoto teaches the gate and control circuit are configured to modulate an electric field within the body to cause the device to transition between a current-conducting state in which the device is in avalanche breakdown condition and a current-blocking state [0071-0091].

Claim 4: Akimoto teaches the control circuit is configured to apply a relatively high bias voltage at the gate to maintain the device in a current-conducting state in which the device is in an avalanche breakdown condition, and apply a relatively low bias voltage at the gate to maintain the device in a current-blocking state [0071-0091].

Claim 5: Akimoto teaches the control circuit is configured to apply the relatively high bias voltage to shorten the effective length of the intermediate region [0071-0091].

Claim 6: Akimoto teaches the control circuit is configured to apply a relatively low bias voltage at the gate to maintain the device in a current-conducting state in which the device is in an avalanche breakdown condition, and a relatively-high bias voltage at the gate to maintain the device in a current-blocking state region [0071-0091].

Claim 7: Akimoto teaches the control circuit is configured to apply the relatively low bias voltage to shorten the effective length of the intermediate region [0071-0091].

Claim 9: Akimoto teaches the gate is located at least predominantly over the intermediate region (FIG. 1A-1B; [0071-0072]).

Claim 10: Akimoto teaches the gate is located to provide a surface channel nearer the second junction than the first junction (FIG. 1A-1B; [0071-0072]).

Claim 11: Akimoto teaches wherein when the body is reversed- biased, the control circuit is configured to apply the control signal to maintain the first region at a relatively lower voltage level than the second region, the difference in potential of the first and second regions being sufficient to cause a breakdown condition in the intermediate region in response to the control signal modulating the length of the intermediate region and thereby reducing the distance across the intermediate region over which the potential drops [0071-0091].

Claim 12: Akimoto teaches the intermediate region has a polarity that is neutral relative to the polarity of the first and second regions (FIG. 1A-1B; [0071-0072]).

Claim 13: Akimoto teaches the intermediate region is lightly doped to achieve the polarization of one of the first and second regions, the intermediate region having a substantially lower dopant concentration level, relative to said one of the first and second regions (FIG. 13).

Claim 14: Akimoto teaches the intermediate region is substantially intrinsic (FIG. 1A-1B; [0071-0072]).

Claim 15: Akimoto teaches the control circuit and gate are further adapted to cause the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state in which substantially no leakage current passes between the first and second regions [0071-0091].

Claim 16: Akimoto teaches the control circuit is configured for applying the control signal to change the concentration of carriers in the intermediate region [0071-0091].

Claim 17: Akimoto teaches the control circuit and gate are further adapted to increase an electric field in the intermediate region and for causing an avalanche breakdown condition (FIG. 1A-1B; [0071-0072]).

Claim 18: Akimoto teaches a semiconductor device comprising:

a multi-region body including a P-type region (23), an N-type region (22) and an intermediate region (20) having a first junction with the P-type region and a second junction with the N-type region, the body adapted to be reverse biased across the P-type and N- type regions;

a gate (20) coupled via an intervening gate dielectric material to the intermediate region, located over one of the junctions and laterally offset from the other junction to present an electric field substantially at only one of the two junctions(FIG. 1A-1B; [0071-0072]).

a control circuit configured to apply a voltage-bias control signal to the gate to control the gate, the P-type region and the N-type region to switch the device between at least two stable conductance states (Fig. 3A-3B [0076-0091]).

Claim 19: Akimoto teaches the control circuit applies the voltage-bias control signal to the gate to switch the device between a high-resistance conductance state and a low-resistance conductance state by causing an avalanche breakdown condition at a field-induced junction in the intermediate region [0071-0091]

Claim 20: Akimoto teaches the intermediate region has a length that separates the first and second junctions sufficiently to permit the avalanche breakdown condition before another breakdown condition when the body is reverse biased (FIG. 1A-1B; [0071-0072]).

Claim 30: Akimoto teaches a memory circuit comprising: a data storage node; first and second multi-region bodies, each body including a first region dominated by charge carriers of a first polarity that extends to a first junction, a second region dominated by charge carriers of a second polarity opposite the first polarity that extends to a second junction, and an intermediate region having an effective length extending from the first junction to the second junction; a first gate coupled to the first multi-region body via an intervening dielectric material and offset for using a control signal, when the first body is reversed biased, to present an electric field substantially at only one of the first and second junctions of the first body, a second gate coupled to the data storage node and to the second body via an intervening dielectric material and adapted for using a charge at the data storage node, when the second body is reversed biased, to modulate an electric field in the intermediate region of the second body, the second body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the second body is in an avalanche breakdown condition and current passes through the second body (FIG. 1-9, 18; [0061-0148, 0231-0243])

a control circuit configured to apply said control signal to the first gate, when the first body is reversed biased, to cause the first body to respond to the electric (Fig. 3A-3B [0076-0091]).

Claim 31: Akimoto teaches a sense device coupled to the second body and adapted to detect data as a function of sensed current passing through the second body, and wherein the second gate is further adapted to influence an electric field substantially at only one of the first and second junctions ((FIG. 1-9, 18; [0061-0148, 0231-0243])

Claim 32: Akimoto teaches a semiconductor device, comprising: a multi-region body including a first region (142) dominated by charge carriers of a first polarity that extends to a first junction, a second region (143) dominated by charge carriers of a second polarity opposite the first polarity that extends to a second junction, and an intermediate region (144) having an effective length extending from the first junction to the second junction;

first (140) and second (141) gates coupled to the body via intervening dielectric material (FIG. 15; [0071-0072; 00197-0201]).

a control circuit configured to apply control signals, when the body is reversed biased to the first and second gates to present an electric field substantially at one of the first and second junctions, to cause the body to respond to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition (Fig. 3A-3B [0076-0091]).

Claim 33: Akimoto teaches the control circuit is configured to apply a control signal to the first gate to capacitively couple a first voltage-bias control signal to the body to accumulate carriers immediately adjacent to said one of the first and second junctions, and to hold the body in a steady state without the avalanche breakdown condition occurring absent a similarly-biased control signal capacitively coupled to the body from the second gate [0071-0091].

Claim 34: Akimoto teaches the control circuit is configured to apply a control signal to the first gate to capacitively couple a first voltage-bias control signal to the body to accumulate carriers immediately adjacent to said one of the first and second junctions, and to switch the body the current-conducting state by applying a second voltage-bias control signal capacitively coupled to the body, the first and second voltage-bias control signals being of similar bias [0071-0091].

Claim 35: Akimoto teaches the control circuit is responsive to temperature and configured to apply a control signal to the body via the second gate to counter temperature-related effects that alter the creation of the avalanche breakdown condition in response to a control signal being applied by the first gate [0071-0091].

Claim 36: Akimoto teaches the control circuit is configured to apply the control signal to the second gate to maintain a threshold voltage level in the intermediate region, the threshold voltage being a minimum amount of additional voltage applied to the intermediate region for causing the avalanche breakdown condition [0071-0091].

Claim 37: Akimoto teaches an inverter circuit comprising: first (44) and second (43) multi-region bodies, each body having a highly-doped P-type region (23p) that

extends to a first junction, a highly-doped N-type region (22p) that extends to a second junction, and an intermediate region (24p) having a neutral polarity relative to the P-type and N-type regions and having a length extending from the first junction to the second junction, the N-type region of the first body and the P-type region of the second body being coupled to a common output node; first (20p) and second (20p) gates respectively capacitively coupled to the first and second bodies (FIG. 1-9, 18; [0061-0148, 0231-0243]).

a control circuit configured to apply control signals to the first and second gates when the bodies are reversed biased, to modulate the length of the intermediate regions of the respective bodies by changing a concentration of carriers in the respective intermediate regions at one of the junctions and offset from the other junction; and an input node coupled to the first and second gates, wherein a change in input signal applied to the input nodes causes an inverted response in an output signal at the output node (Fig. 3A-3B [0076-0091]).

Claim 38: Akimoto teaches a semiconductor device comprising: a relatively thin intermediate region defined by sides including an upper portion and a sidewall portion; a first region dominated by a first polarization that extends to a first junction with the intermediate region; a second region dominated by a second polarization that extends to a second junction with the intermediate region; and a gate extending around and capacitively coupled to at least two sides of the intermediate region for coupling a voltage to the intermediate region (Fig. 17).

a control circuit including a gate coupled to the body via an intervening dielectric material and offset for applying a control signal via the gate, when the body is reversed biased to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body. Akimoto teaches a control circuit including a gate coupled to the body via an intervening dielectric material and offset for applying a control signal via the gate, when the body is reversed biased to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body to improve device operation (Fig. 3A-3B; ABS, [0076-0091]).

Claim 39: Akimoto teaches a semiconductor device, comprising: a multi-region body including a first region (22) dominated by charge carriers of a first polarity that extends to a first junction, a second region (23) dominated by charge carriers of a second polarity opposite the first polarity that extends to a second junction, and an intermediate region (24) having an effective length extending from the first junction to the second junction; and (FIG. 1A-1B; [0071-0072]).

a gate and a control circuit for presenting, when the body is reversed biased, an electric field at the first junction and offset from the second junction, the body responding to the electric field by switching from a stable conductance state to a

current-conducting state in which the body is in an avalanche breakdown condition and current passes in the body (Fig. 3A-3B [0076-0091]).

Claim 43: Akimoto teaches a semiconductor device, comprising: a multi-region body having an upper surface and including a first region (22) dominated by carriers of a first polarity that extends to a first junction, a second region (23) dominated by carriers of an opposite polarity that extends to a second junction, and an intermediate region (24) having an upper portion over a lower portion and a length extending from the first junction to the second junction; a gate (20) capacitively-coupled to the body (FIG. 1A-1B; [0071-0072]).

a control circuit configured for applying a control signal to the gate, when the body is reversed biased, to cause the gate to modulate the length of the intermediate region by changing a concentration of carriers in a portion of the intermediate region extending from one of the junctions and offset from the other of the junctions and thereby causing the device to transition between a current-conducting state in which the device is in an avalanche breakdown condition and a current-blocking state the avalanche breakdown condition occurring in the lower portion of the intermediate region, the upper portion of the intermediate region being arranged to inhibit hot carriers from the lower portion reaching the upper surface in a current-conducting state (Fig. 3A-3B [0076-0091]).

Claim 44: Akimoto teaches the control circuit is configured with the body and gates, to apply the control signals to operate the body under subthreshold conditions leading up to switching of the device between the stable and current-conducting states,

in which the subthreshold slop pertaining to a change in current per a corresponding change in voltage is significantly lower than about 60mV/decade.

Claim 45: Akimoto teaches an impact ionization-based semiconductor device, comprising: a multi-region body including a first region, dominated by charge carriers of a first polarity, that extends to a first junction, a second region, dominated by charge carriers of a second polarity opposite the first polarity, that extends to a second junction, and an intermediate region having an effective length extending from the first junction the to the second junction; first and second gates coupled to the body via intervening dielectric material (FIG. 15; [0071-0072; 00197-0201]).

a control circuit configured to apply control signal, when the body is reversed biased, to the respective first and second gates to generate an electric field substantially at one of the first and second junctions, and to cause the body to switch from a stable conductive state to a current-conducting state in which the body is in an avalanche breakdown condition (Fig. 3A-3B [0076-0091]).

9. Regarding claims 2-7, 9-20, 30-39 and 43-45, the claim limitations with respect to the device transitioning between states and the effective length of the intermediate region changing are mainly directed to the intended use of the transistor and since performing said functions would involve merely manipulating the voltages applied to the gate and as mentioned above in paragraph 8.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto (US PGPub 2002/0117689), as applied to claim 1 above, and further in view of Baba (US Patent 5,589,696 of record).

Regarding claim 8, as described above, Akimoto substantially reads on the invention as claimed, except Akimoto does not teach the gate is located at least predominantly over the second region. Baba ('696) teaches the gate (21) is located at least predominantly over the second region (FIG. 2) to be more highly integrated (Col. 4 lines 1-20). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Akimoto, Baba ('739) and Yee to have the gate located predominantly over the second region to be more highly integrated as taught by Baba ('696) (Col. 4 lines 1-20).

11. Claims 21-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizutani (US Patent 5,616,944 of record) in view of Akimoto (US PGPub 2002/0117689 of record).

Claim 21: Mizutani teaches a memory circuit comprising: a data storage node; a multi-region body including a first region dominated by charge carriers of a first polarity that extends to a first junction, a second region dominated by charge carriers having a second and opposite polarity that extends to a second junction, and an intermediate region having an effective length extending from the first junction to the second junction, the gate being coupled to the body via an intervening dielectric material (FIG. 1; Col. 3-5).

Mizutani does not teach a control circuit including a gate coupled to the body via an intervening dielectric material and offset for applying a control signal via the gate, when the body is reversed biased to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body. Akimoto teaches a control circuit including a gate coupled to the body via an intervening dielectric material and offset for applying a control signal via the gate, when the body is reversed biased to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body to improve device operation (Fig. 3A-3B; ABS, [0076-0091]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Mizutani to have the gate coupled to the body in an offset matter in conjunction with a control circuit to improve device operation as taught by Akimoto (ABS).

12. Akimoto and Mizutani do not specifically teach the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body. Akimoto and Mizutani, however, do teach all aspects of the semiconductor device structure in accordance with the instant claimed

invention and body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body is a function that does not affect the structure of the final device. Furthermore, Akimoto and Mizutani's device is capable of performing the claimed functions. For instance, manipulating the bias applied to the gate and diffusion regions of the device taught by Akimoto and Mizutani will result in the body switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body.

Claim 22: Mizutani (FIG. 1; Col. 3-5) and Akimoto ([0071-0091] teach the body and the control circuit are adapted to access data stored at the data storage node as a function of the avalanche breakdown condition.

Claim 23: Mizutani (FIG. 1; Col. 3-5) and Akimoto ([0071-0091] teach the body and the control circuit are adapted to read data from the data storage node as a function of the avalanche breakdown condition.

Claim 24: Mizutani (FIG. 1; Col. 3-5) and Akimoto ([0071-0091] teach the body and the control circuit are configured to write data to the data storage node as a function of the avalanche breakdown condition.

Claim 25: Mizutani (FIG. 1; Col. 3-5) and Akimoto ([0071-0091] the control circuit maintains a charge at the data storage node by applying the control signal to control the body in a reverse biased condition.

Claim 26: Mizutani teaches the body and the storage nodes are adapted to drain a charge at the storage node in response to the body being placed in a forward biased condition (FIG. 1; Col. 3-5).

Claim 27: Mizutani teaches a memory circuit comprising: a data storage node; a multi-region body including a first region dominated by charge carriers having a first polarization that extends to a first junction, a second region dominated by charge carriers having a second polarity that is opposite the first polarity that extends to a second junction, and an intermediate region having an effective length extending from the first junction to the second junction (FIG. 1; Col. 3-5).

Mizutani does not teach a control circuit including a gate coupled to the body via an intervening dielectric material and offset for applying a control signal via the gate, when the body is reversed biased to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body. Akimoto teaches a control circuit including a gate coupled to the body via an intervening dielectric material and offset for applying a control signal via the gate, when the body is reversed biased to present an electric field substantially at only one of the first and second junctions, the body responding to the electric field by switching from a stable conductance state to a current-conducting state in which the body is in an avalanche breakdown condition and current passes between the data storage node and the body to improve device operation (Fig. 3A-3B; ABS, [0076-0091]). Therefore it

would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Mizutani to have the gate coupled to the body in an offset matter in conjunction with a control circuit to improve device operation as taught by Akimoto (ABS).

Claim 28: Mizutani teaches the data storage node is coupled to the gate, the gate responding to a charge at the data storage node by presenting the electric field (FIG. 1; Col. 3-5).

Claim 29: Mizutani teaches a sense device coupled to the body and adapted to detect data stored at the data storage node in response to current passing through the body (FIG. 1; Col. 3-5).

13. Regarding claims 21-29, the claim limitations with respect to the device transitioning between states and holding/draining charge are mainly directed to the intended use of the transistor and since performing said functions would involve merely manipulating the voltages applied to the gate and as mentioned above in paragraph 12.

Response to Arguments

14. Applicant's arguments with respect to claims 1-39 and 43-45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarah K Salerno whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. K. S./
Examiner, Art Unit 2814

/Marcos D. Pizarro/
Primary Examiner, Art Unit 2814